Please replace the paragraph starting on line 33 of page 9 of the specification with the following amended paragraph.

a4 The sub reset signal generators 10 and 12 and pulse generators 16 and 18 are the same as those of the first embodiment. The pulse generator 38 is the same as the pulse generator 16. The composite circuit 40 is constructed of a negative logic OR circuit. The composite circuit 40 receives pulses PLSH, PLSL and PLSE and generates a power-on reset signal POR.

Pursuant to 37 C.F.R. § 1.121, as amended, a copy of the marked-up version of the original paragraphs is attached to this Response showing the changes made therein.

IN THE CLAIMS:

Please amend claims 1-7 as follows. Pursuant to 37 C.F.R. § 1.121, as amended, a copy of the marked-up version of the original claims is attached to this Response showing the changes made therein.

a5 SUB C1 1. (Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one from any of said sub power-on reset signals.

SUB B1 2. (Amended) A semiconductor integrated circuit according to claim 1, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for corresponding one of said sub power-on reset signals; and

a composite circuit for synthesizing the pulses to generate said main power-on reset signal.

3. (Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a sub power-on reset signal;

a reset terminal for receiving an external power-on reset signal; and

a main reset signal generator for generating a pulse signal as a main power-on reset signal to initialize an internal circuit, according to at least one of said sub power-on reset signal and said external power-on reset signal.

4. (Amended) A semiconductor integrated circuit according to claim 3, wherein said main reset signal generator comprises:

a plurality of pulse generators for respectively generating pulses on the basis of a transition edge for corresponding one of said sub power-on reset signal and said external power-on reset signal; and

a composite circuit for synthesizing said pulses to generate said main power-on reset signal.

5. (Amended) A semiconductor integrated circuit comprising:

a sub reset signal generator for generating a plurality of sub power-on reset signals at timings different from each other;

a reset terminal for receiving an external power-on reset signal; and